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**Xie et al.**

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(54) **RESIST HARDENING AND DEVELOPMENT PROCESSES FOR SEMICONDUCTOR DEVICE MANUFACTURING**

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CPC . ***G03F 7/405*** (2013.01); ***G03F 7/36*** (2013.01)

(58) **Field of Classification Search**
CPC ..... G03F 7/26
See application file for complete search history.

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(57) **ABSTRACT**

In some embodiments, a method of forming an etch mask on a substrate is provided that includes (1) forming a resist layer on a substrate; (2) exposing one or more regions of the resist layer to an energy source so as to alter at least one of a physical property and a chemical property of the exposed regions; (3) performing a hardening process on the resist layer to increase the etch resistance of first regions of the resist layer relative to second regions of the resist layer, the hardening process including exposing the resist layer to one or more reactive species within an atomic layer deposition (ALD) chamber; and (4) dry etching the resist layer to remove the one or more second regions and to form a pattern in the resist layer. Other embodiments are provided.

**18 Claims, 5 Drawing Sheets**